iU6395

3-Phase BLDC Motor Controller

Preliminary Datasheet Rev. P0.1

1. Description

The iU6395 is a 3-phase BLDC motor controller IC integrated with various peripherals to realize sensor or sensor-less BLDC motors application, including FOC. The iU6395 is embedded with 3-phase N/N MOS pre-driver. The logic input is compatible with standard CMOS output. It features the flexibility to adjust various motor parameters and complete protection such as over current, over voltage and under voltage lockout.

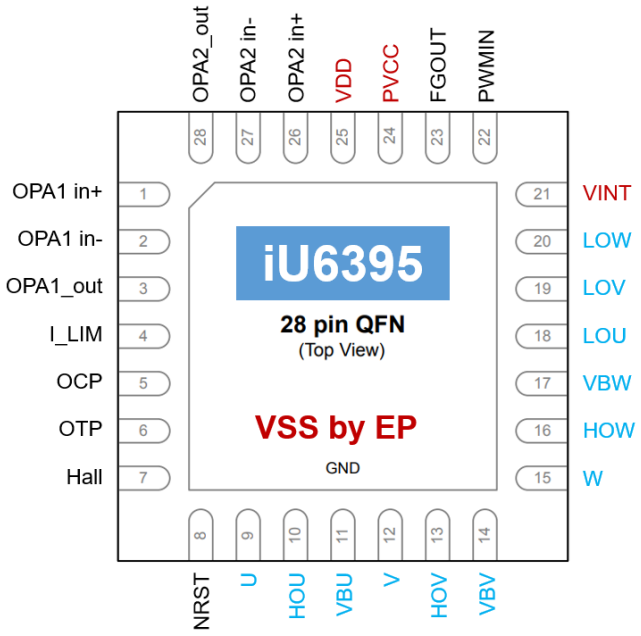
2. Features

- 3-Phase BLDC Motor Controller with N/N MOS Pre-driver
- Embedded with
  - ✓ 5V Regulator Output (VDD) for Hall Sensor
  - ✓ 8V Regulator Output (VINT) for External MOSFET Gate Driver Voltage
  - ✓ Max. 20V N/N MOS Pre-driver
  - ✓ Internal Current Amplifier x 2
- Control Functions
  - ✓ Support PWM duty and Clock input
  - ✓ FG Output (customized waveform is feasible)
  - ✓ Adjustable Start
  - ✓ Initial Brake
  - ✓ Constant Power
  - ✓ Windmill Startup Operation
  - ✓ Setting RPM maximum limit by open loop
- Built-in Protection
  - ✓ Over-Voltage
  - ✓ Over-Current
  - ✓ Current Limit
  - ✓ Over Temperature (internal thermal sensor and external sensor pin)
  - ✓ Auto Recovery
- 4-wire programming
- QFN-28 4x4 Package

3. Applications

- BLDC Motor Driver

4. Pin Assignments



5. Marking Information

Product Name	Marking
iU6395	 X: Date code

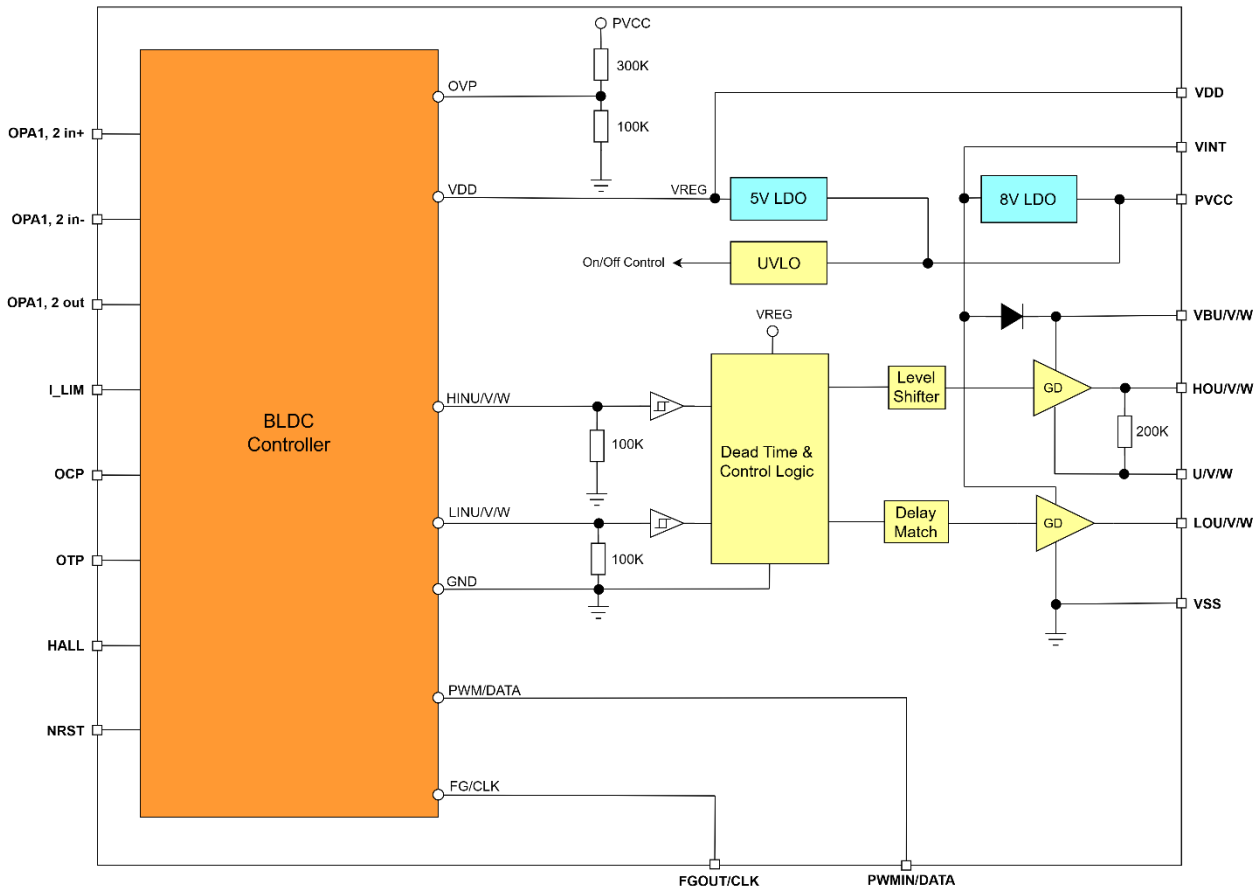
6. Ordering Code

Ordering Code
iU6395

7. Pin Definitions

Pin No.	Symbol	Pin Group	Description
1	OPA1 in+	I/O	OPAMP1 Positive Input
2	OPA1 in-	I/O	OPAMP1 Negative Input
3	OPA1_out	I/O	OPAM1 Output
4	I_LIM	I/O	Average Current Detection
5	OCP	I/O	Over Current Protection
6	OTP	I/O	Over Temperature Protection
7	HALL	I/O	Hall
8	NRST	I/O	External RESET
9	U	Power	U-phase, High side floating supply return
10	HOU	Power	U-phase, High side gate driver
11	VBU	Power	U-phase, High side floating supply
12	V	Power	V-phase, High side floating supply return
13	HOV	Power	V-phase, High side gate driver
14	VBV	Power	V-phase, High side floating supply
15	W	Power	W-phase, High side floating supply return
16	HOW	Power	W-phase, High side gate driver
17	VBW	Power	W-phase, High side floating supply
18	LOU	Power	U-Phase, Low Side Gate Driver
19	LOV	Power	V-Phase, Low Side Gate Driver
20	LOW	Power	W-Phase, Low Side Gate Driver
21	VINT	Power	8V Regulator Output for Pre-Driver
22	PWMIN / DATA	HV I/O	PWM/VSP input (for Flash Write, DATA)
23	FGOUT / CLK	HV I/O	FG Output (for Flash Write, CLK)
24	PVCC	Power	Power VCC Supply
25	VDD	Power	Self 5V Logic Power
26	OPA2 in+	I/O	OPAMP2 Positive Input
27	OPA2 in-	I/O	OPAMP2 Negative Input
28	OPA2_out	I/O	OPAMP2 Output
EP	VSS	Power	Ground

8. Function Block Diagram



9. Electrical Characteristics

9.1 Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to VSS (GND), all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Parameter	Min.	Max.	Unit
PVCC	Power VCC Supply	-0.3	22	V
VDD	Voltage of 5V LDO Output	-0.3	5.8	V
VINT	Voltage of 8V LDO Output	-0.3	9.5	V
$V_{HOU,V,W}$	Voltage of High Side Gate Driver Output	$V_{U,V,W}$ - 0.3	$VB_{U,V,W}$ + 0.3	V
$V_{LOU,V,W}$	Voltage of Low Side Gate Driver Output	-0.3	VINT + 0.3	V
$VB_{U,V,W}$	Bootstrap Voltage to High Side Gate Driver	$V_{U,V,W}$ - 0.3	$V_{U,V,W}$ + VINT	V
$V_{U,V,W}$	Voltage of Return Path for High Side Gate Driver	-0.3	22	V
V_{FGOUT}	Voltage of FG Output (for Flash Write, CLK)	-0.3	22	V
V_{PWMIN}	Voltage of PWM/VSP input (for Flash Write, DATA)	-0.3	22	V
I/O Pin	Logic Input Voltage	- 0.3	5.5	V
Tj	Junction Temperature (Note)	-40	125	℃
T_S	Storage Temperature	-55	150	

Note: Please do not exceed Tj limitation

In the following electrical characteristics, the parameter given in the table below is derived from the tests performed under general operation conditions and room temperature, unless special bias or temperature condition is specified.

9.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
PVCC	Power VCC Supply	5	18	V
$VB_{U,V,W}$	Bootstrap Voltage to High-side Gate Driver	$V_{U,V,W}$ – 0.3	$V_{U,V,W}$+ VINT	V
$V_{U,V,W}$	Voltage of Return Path for High Side Gate Driver	-0.3	18	V
V_{FGOUT}	Voltage of FG Output (for Flash Write, CLK)	0	18	V
V_{PWMIN}	Voltage of PWM/VSP input (for Flash Write, DATA)	0	18	V
I/O Pin	Logic Input Voltage	0	VDD	V
T_A	Ambient Temperature (Note)	-40	105	℃

Note: Please do not exceed Tj limitation.

9.3 D.C. Characteristics

Symbol	Conditions			Min.	Typ.	Max	Unit
	Mode	f_{HCLK}	Conditions				
IDD*	Operation Mode Internal Clock	60MHz	All Peripherals Enabled	-	8.61	-	mA
			All Peripherals Disabled	-	7.08	-	mA
		40KHz	All Peripherals Enabled	-	1.02	-	mA
			All Peripherals Disabled	-	1.00	-	mA
	Sleep Mode, Internal Clock	60MHz	All Peripherals Enabled	-	3.52	-	mA
			All Peripherals Disabled	-	2.25	-	mA
		40KHz	All Peripherals Enabled	-	1.00	-	mA
			All Peripherals Disabled	-	1.00	-	mA
	Stop Mode	-	Enter Stop Mode after Reset	-	110	-	uA

* Only BLDC controller, gate driver is not included.

9.4 A.C. Characteristics

9.4.1 High Speed Internal Oscillator (HSI) Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
f_{HSI}	Frequency	-	-	60	-	MHz
ACC_{HSI}	Accuracy of HSI Oscillator	T_A = -40°C ~ 105°C	-2.5	-	+2.5	%
		T_A = -10°C ~ 85°C	-1.5	-	+1.5	%
		T_A = 25°C	-1	-	+1	%

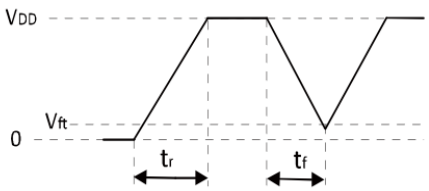
9.4.2 Low Speed Internal Oscillator (LSI) Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
F_{LSI}	Frequency	T_A = -40°C ~ 105°C	20	40	60	KHz
$tsu_{(LSI)}$	LSI Oscillator Start-up Time	-	-	-	300	us
$IDD_{(LSI)}$	Power Consumption of LSI Oscillator	-	-	0.34	-	uA

9.4.3 Power-up and Power-down Characteristics

Symbol	Conditions	Min.	Typ.	Max	Unit
t_{VDD}	VDD Rising Time tr	300	-	50000	us
	VDD Falling Time tf	300	-	50000	
V_{ft}	Power-down Threshold Voltage	0	-	-	mV

Note 1：Derived from overall evaluation, not tested in production.
Note 2：The on-chip VDD waveform during power-down should follow the tr and tf stages as shown in the waveform diagram below.
Note 3：The chip should be powered up from 0V to ensure reliable power-up.
Note 4：VDD means LDO5V for BLDC controller power supply.



9.4.4 Low-Power Mode Wake-up Time

Symbol	Conditions	Min.	Typ.	Max	Unit
$t_{WUSLEEP}$	Wake-up from Sleep Mode (System Clock is HSI)	-	1.5	-	us
t_{WUSTOP}	Wake-up from Stop Mode (System Clock is HSI)	-	65	-	us

9.5 Input / Output Characteristics

9.5.1 Standard I/O

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
V_{IL}	Input low-level voltage	5V CMOS port	-	-	0.3 * VDD	V
V_{IH}	Input high-level voltage	5V CMOS port	0.7 * VDD	-	-	V
V_{hy}	I/O pin Schmitt trigger voltage hysteresis	5V	0.1 * VDD	0.60	-	V
V_{OL}	Output low level	$\|I_{IO}\|$ = 6mA · VDD = 5V		0.11		V
V_{OH}	Output high level			4.83		V
V_{OL}	Output low level	$\|I_{IO}\|$ = 8mA · VDD = 5V		0.15		V
V_{OH}	Output high level			4.78		V
V_{OL}	Output low level	$\|I_{IO}\|$ = 20mA · VDD = 5V		0.38		V
V_{OH}	Output high level			4.4		V
I_{lkg}	Input leakage current	5V	-1	-	1	μA
R_{PU}	Weak pull-up equivalent resistor	Vinput= VSS	50	60	75	kΩ
R_{PD}	Weak pull-down equivalent resistor	Vinput= 5V	50	60	75	kΩ
C_{IO}	I/O pin capacitance	-	-	-	10	pF

Note：VDD means LDO5V for BLDC controller power supply.

9.5.2 HV I/O

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
I_{LK_FGOUT}	Off State Leakage	V_{FGOUT} = 18V			1.0	μA
V_{FGOUT}	On State	I_{FGOUT} = 10mA		0.16	0.2	V
I_{LK_PWMIN}	Off State Leakage	V_{PWMIN} = 18V			1.0	μA
V_{IL_PWMIN}	Input low-level voltage				1.0	V
V_{IH_PWMIN}	Input high-level voltage		2.1			V

9.6 POR / PVD Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
V_{PVD}	Level Selection for Programmable Voltage Detector	Rising Edge: Level 1	-	2.4	-	V
		Falling Edge: Level 1	-	2.3	-	V
		Rising Edge: Level 2	-	2.7	-	V
		Falling Edge: Level 2	-	2.6	-	V
		Rising Edge: Level 3	-	3.0	-	V
		Falling Edge: Level 3	-	2.9	-	V
		Rising Edge: Level 4	-	3.3	-	V
		Falling Edge: Level 4	-	3.2	-	V
		Rising Edge: Level 5	-	3.6	-	V
		Falling Edge: Level 5	-	3.5	-	V
		Rising Edge: Level 6	-	3.9	-	V
		Falling Edge: Level 6	-	3.8	-	V
		Rising Edge: Level 7	-	4.2	-	V
		Falling Edge: Level 7	-	4.1	-	V
		Rising Edge: Level 8	-	4.5	-	V
		Falling Edge: Level 8	-	4.4	-	V
		Rising Edge: Level 9	-	4.8	-	V
		Falling Edge: Level 9	-	4.7	-	V
V_{POR}	Power-on Reset Threshold	-	-	2.2	-	V
$V_{hyst\_POR/PDR}$	POR/PDR Hysteresis	-	-	60	-	mV
$T_{RSTTEMPO}$	Reset Duration	-	-	1.84	-	ms

9.7 A/D Converter Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
f_{ADC}	ADC Clock Frequency	VDD ≥ 2.5V	-	-	15	MHz
f_S	Sampling Rate	12bits; VDD ≥ 2.5V	-	-	1	MHz
f_{TRIG}	External trigger frequency	12bits; f_{ADC} = 15MHz	-	-	1	MHz
		12bits	-	-	15	1/ fADC
R_{AIN}	External Input Impedance	-	See the formula below			KΩ
R_{ADC}	Sampling switch resistance	-	-	-	1.5	KΩ
C_{ADC}	Internal sampling and holding capacitance	-	-	-	5	pF
t_{STAB}	Power-up Time	-	-	-	10	μS
t_{lat}	Injection-Trigger Conversion Delay	-	-	-	512	1/fADC
t_{latr}	Regular-Trigger Conversion Delay	-	-	-	512	1/fADC
ts	Sampling Time	f_{ADC} = 15MHz	0.167	-	16.03	μS
t_{CONV}	Total Conversion Time (including Sampling Time)	12bits; f_{ADC}=15MHz	1	-	16.87	μS
ENOB	Effective Number of Bits	12bits; VDD ≥ 3.3V; f_{ADC} = 15MHz	-	10.9	-	bit

Note 1：For external triggering, a delay of 1/f_{ADC} must be added to the timing

Note 2：VDD means LDO5V for BLDC controller power supply.

Symbol	Parameter	Conditions	Typ.	Unit
ET	Overall Error	f_{PCLK1}=60MHz, f_{ADC}=15MHz, R_{AIN}<0.1KΩ, VDD=5V, T_A=25°C	-4.7 to +3.4	LSB
EO	Offset Error		-1.9 to +2.8	LSB
EG	Gain Error		-0.4 to +1.6	LSB
ED	Differential Linearity Error		-1.0 to +0.4	LSB
EL	Integral Linearity Error		-2.2 to +3.4	LSB

Note：VDD means LDO5V for BLDC controller power supply.

9.8 Operational Amplifier Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
V_{DD}	Supply Voltage	-	2.5	-	5.5	V
V_{OFFSET}	Input Bias Voltage	-	-	1	-	mV
I_{LOAD}	Drive Current	Drive current (sinking current) (VDD=5V, VOUT=1V)	-	-	15	mA
C_{LOAD}	Capacitive Load	-	-	-	30	pF
CMRR	Common Mode Rejection Ratio	-	-	80	-	dB
PSRR	Power Supply Rejection Ratio	-	-	80	-	dB
GBW	Gain-Bandwidth Product	-	-	12	-	MHz
SR	Slew Rate	-	-	7	-	V/us
GOL	Open-loop Gain	-	90	110	120	dB

Note: VDD means LDO5V for BLDC controller power supply.

9.9 Comparator Electrical Characteristics

Symbol	Parameter	Register Configuration	Min.	Typ.	Max	Unit
t_{HYST}	Hysteresis	00(hysteresis), high power	-	0	-	mV
		00(hysteresis), low power	-	0	-	mV
		01(hysteresis), high power	15	22	43	mV
		01(hysteresis), low power	13	15	23	mV
		10(hysteresis), high power	32	45	92	mV
		10(hysteresis), low power	25.2	32	46.7	mV
		11(hysteresis), high power	55	85	182	mV
		11(hysteresis), low power	25.5	60	83.9	mV
V_{OFFSET}	Offset Voltage	-		+/-6	+/-10.4	mV
t_{DELAY}	Propagation Delay Note1	00（high power）	3.7	10.7	43	ns
		01（medium power）	10.5	34.9	83	ns
		10（low power）	13.8	49	114	ns
		11（ultra-low power）	22.2	86	194.5	ns
Iq	Average Operating Current	00（high power）	6.5	45	205.4	μA
		01（medium power）	3.3	21.7	81.3	μA
		10（low power）	2.6	15.3	59.6	μA
		11（ultra-low power）	1.7	8.8	35.3	μA

Note1 : Time difference between 50% output transition and input transition.

9.10 Gate-driver Electrical Characteristics

(Ta = 25°C, PVCC= $VB_{U,V,W}$ = 12V, $V_{U,V,W}$=VSS=GND, C_{Load} = 1000pF)

Symbol	Description	MIN	TYP	MAX	Unit
Dynamic Parameters					
ton	Turn-on Delay Time	-	120	200	ns
toff	Turn-off Delay Time	-	120	200	ns
tr	Rising Time	-	140	200	ns
tf	Falling Time	-	55	100	ns
MTon	Matching Turn-on Propagation Delay Time for the Same Phase High-Side & Low-Side	-	-	50	ns
MToff	Matching Turn-on Propagation Delay Time for the Same Phase High-Side & Low-Side	-	-	50	ns
PDD	PWM Duty Distortion (Note)	-	--	10	%
tDT	Dead Time	150	200	300	ns
Static Parameters					
VOH	High Level Output Voltage, IO = -20mA (Low side : VINT-VLO, High side: VBS-VHO)	-	-	0.3	V
VOL	Low Level Output Voltage, IO = +20mA	-	-	0.2	V
IQCC	VCC Quiescent Current, HO & LO = Low	-	-	0.8	mA
IQBS	VBS Quiescent Current, HO = Low	-	30	60	uA
ILK	VS Leakage Current	-	-	10	uA
IO+	Driver Sourcing Peak Current	-	0.7	-	A
IO-	Driver Sinking Peak Current	-	1.0	-	A
$VCC_{UVLO\ ON}$	PVCC UVLO Voltage	4.0	4.8	5.5	V
HYS_VCC	PVCC UVLO Hysteresis	-	0.2	-	V
$VBS_{UVLO\ ON}$	VBS UVLO Voltage	4.0	4.8	5.5	V
HYS_VBS	VBS UVLO Hysteresis	-	0.2	-	V
V_BSD	Bootstrap Diode Conduction Voltage Drop	-	0.7	1	V
R_BSD	Bootstrap Diode Equivalent Resistance	-	180	320	Ω

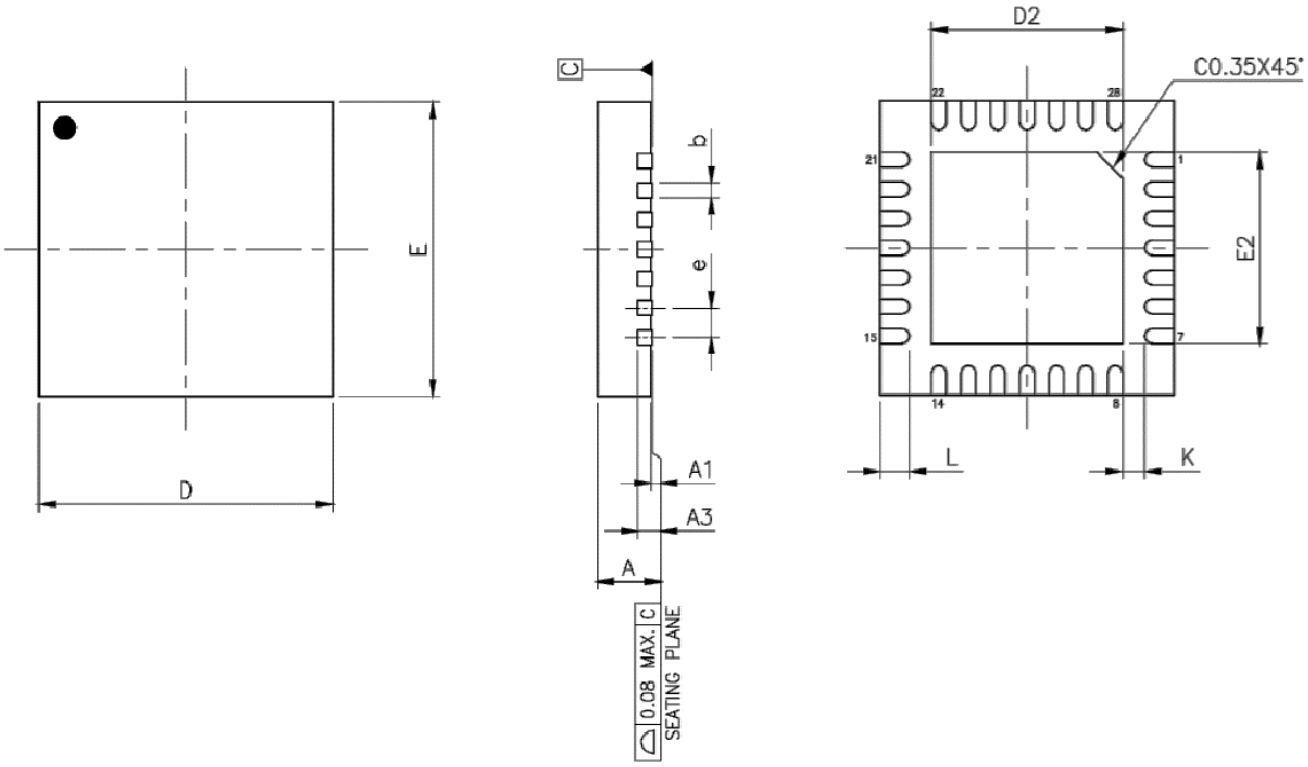
Note: The PWM duty distortion is Hin / Lin > 1us, HO duty distortion = ±10%.

9.11 LDO Electrical Characteristics

Symbol	Description	MIN	TYP	MAX	Unit
VDD	Internal 5V LDO Voltage (PVCC=5.5~20V, IDD=30mA, C_{VDD}=1uF)	4.75	5	5.25	V
	Internal 5V LDO Voltage (PVCC=5V, IDD=15mA, C_{VDD}=1uF)	4.5			V
VINT	Internal 8V LDO Voltage (PVCC=10~20V, IVINT=30mA, C_{VINT}=1uF)	7.6	8	8.4	V
	Internal 8V LDO Voltage (PVCC=5V, IVINT=15mA, C_{VINT}=1uF)	4.5			V
VDD_LineReg	5V LDO Line Regulation △VDD (IO = 1 mA, 7.5V ≤ PVCC ≤ 12.7V)		50		mV
VDD_LoadReg	5V LDO Loading Regulation △VDD (1mA ≤ Io ≤ 30mA, PVCC=12V)		100		mV
VDD_Drop	5V LDO Dropout Voltage (IO=20 mA, PVCC=5V)		0.5	1.0	V
I_{VDD_Lim}	5V LDO Output Current Limit, PVCC=12V		50		mA
VINT_LineReg	8V LDO Line Regulation △VINT (IO = 1 mA, 8.5V ≤ PVCC ≤ 12.7V)		50		mV
VINT_LoadReg	8V LDO Load Regulation △VINT (1mA ≤ Io ≤ 30mA, PVCC=12V)		100		mV
VINT_Drop	8V LDO Dropout Voltage, (IO = 20 mA, PVCC = 8V)		0.5	1.0	V
I_{VINT_Lim}	8V LDO Output Current Limit, PVCC = 12V		50		mA

10. Package Information

QFN-28 (4.0 x4.0 mm) Outline Dimensions



SYMBOL	Dimension in mm		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.15	0.20	0.30
D		4.00 BSC	
E		4.00 BSC	
e		0.40 BSC	
D2	2.50	2.70	2.90
E2	2.50	2.70	2.90
K	0.20	-	-
L	0.30	0.40	0.50

Important Notice

1. inergy Technology Inc. reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

2. The Products of inergy Technology Inc. have been tested, verified and passed by our specifications and standards, and are 100% inspected before delivery from the factory. It is strongly recommended that the customers shall perform verifications of the functionality, compatibility, and reliability of the environment or platform that you used. inergy Technology Inc. would not be liable for or guarantee anything that is related to the functionality, compatibility, and reliability of the environment or platform used by the customers.